IN THE SPECIFICATION:

Please amend the paragraph beginning on page 1 at line 10 as follows:

--An example of a reproduced signal processing circuit in a conventional optical disk apparatus is shown in FIG. [[**12**]] **23**.--

Please amend the paragraph beginning on page 1 at line 12 as follows:

--In FIG. [[**12**]] **23**, **1** is a recording medium such as an optical disk, **2** is an optical pick-up, **3** is an analog front end, and **12** is a digital signal processing circuit. In the digital signal processing circuit **12** mentioned above, **4** is an A/D converter, **5** is a digital filter, **6** is a decoder, and **13** is a synchronous clock extracting circuit. In the synchronous clock extracting circuit **13** mentioned above, **7** is a phase comparator, **8** and **11** are loop filters, **9** is a VCO (voltage control oscillator), and **10** is a frequency comparator. A description will be given herein below to the detail of the foregoing structure and to the outline of the operation thereof.--

Please amend the paragraph beginning on page 3 at line 1 as follows:

--A conventional structure of the phase comparator **7** in such a synchronous clock extracting circuit is disclosed in, e.g., Japanese Laid-Open Patent Publication No. HEI 8-17145. An example of the conventional structure of the phase comparator **7** will be shown herein below in FIG. [[**13**]] **24**.--

Please amend the paragraph beginning on page 3 at line 11 as follows:

--Subsequently, an example of the conventional structure of the zero cross detecting circuit **74** will be shown in FIG. [[**14**]] **25**. The zero cross detecting circuit **74** in the drawing is composed of an averaging circuit **741**, a D flip-flop **742**, and an EXCUSIVE-OR circuit **743**. The averaging circuit **741** calculates an average value of two consecutive items of reproduced data

and outputs the sign data thereof. The D flip-flop **742** delays the sign data from the averaging circuit **741** by a period corresponding to 1 clock. The sign data EXCLUSIVE-OR circuit **743** receives two sign data items which are the sign data of the average value outputted from the averaging circuit **741** and the sign data delayed in the D flip-flop **742** and detects points at which the signs of the sign data items are inverted from a positive value to a negative value and from a negative value to a positive value. An output from the EXCLUSIVE-OR circuit **743** is used as the zero cross detection signal from the zero cross detecting circuit **74**.--

Please amend the paragraph beginning on page 3 at line 23 as follows:

--An example of the outline of zero cross point detection in the zero cross detecting circuit **74** is shown in FIG. [[**15**]] **26**. The drawing shows the outline of zero cross point detection upon the rising of reproduced data. The circular marks indicate sampling points for the reproduced data, which are represented as a(n-1), a(n), and a(n+1) with a lapse of time. The zero cross point detected as a phase error in this case is a(n). Each of the crossed (X) marks indicates an average value of two consecutive sign data items. Since the average value of the sign data a(n-1) and the subsequent sign data a(n) has a positive sign and the average value of the sign data a(n) and the subsequent sign data a(n+1) has a negative sign, the sign data a(n) in the middle is determined to be the zero cross point. The phase error is calculated based on the value of the sign data a(n) and the direction of a cross edge.--

Please amend the paragraph beginning on page 4 at line 9 as follows:

--The problem of a conventional zero cross detection method is shown in FIGS. [[**16**]] **27**. The drawings show the outline of zero cross detection performed with respect to a (3T + 3T) reproduced waveform (T is a channel cycle period), of which FIG. [[**16(a)**]] **27(a)** shows the outline of zero cross detection that has been performed normally by using the zero cross detection method illustrated with reference to FIG. [[**15**]] **26**. As can be seen from the drawing, a zero cross point is detected correctly when the reproduced data and the sampling clock are in synchronization. By contrast, when a frequency error between the reproduced data and the

sampling clock is large as shown in FIG. [[**16(b)**]] **27(b)**, phase inversion occurs at a given point so that the zero cross point is detected erroneously.--

Please amend the paragraph beginning on page 11 at line 6 as follows:

--In the phase error detecting circuit according to the present invention, the cross reference value generator has, as the reference value for the cross detector, a zero reference value in addition to the reference value based on the threshold from the threshold generator and on the phase error data from the phase error calculator and has a selecting circuit for selecting either one of the zero reference value and the reference value based on the threshold and on the phase error data.--

Please amend the paragraph beginning on page 16 at line 2 as follows:

--FIG. **1** shows a structure of a phase error detecting circuit as a first embodiment of the present invention. The phase error detecting circuit in the drawing is used as a replacement for the phase comparator **7** provided in the synchronous clock extracting circuit **13** of the digital signal processing circuit **12** in the reproduced signal processing circuit in the optical disk apparatus (record reproducing apparatus) shown in FIG. [[**12**]] **23**. Accordingly, the respective structures of the synchronous clock extracting circuit and the reproduced signal processing circuit each having the phase error detecting circuit are the same as in FIG. **12** so that the description thereof will be omitted.--

Please amend the paragraph beginning on page 16 at line 10 as follows:

--In FIG. **1**, **700** is the phase error detecting circuit which detects a phase error from the reproduced data reproduced by the record reproducing apparatus and subjected to AD conversion (quantization) in the A/D converter **4** shown in FIG. **23** and outputs the detected phase error. The phase error detecting circuit **700** is provided in the synchronous clock extracting circuit **13** shown in FIG. [[**12**]] **23** in place of the phase comparator **7** so that phase error data outputted

from the phase error detecting circuit **700** is inputted to the VCO (voltage control oscillator) **9** via the loop filter **8**, as described above, and the VCO **9** changes the frequency of the synchronous clock outputted therefrom in accordance with the phase error of the inputted phase error data.--

Please amend the paragraph beginning on page 27 at line 18 as follows:

--It will easily be appreciated that, for the structure of the control signal generator **73**, a structure which is a combination of the structure in each of the ~~sixth~~ fifth and sixth embodiments and the structure in each of the seventh and eighth embodiments may also be adopted.--